**Motivations**
- Physical limitations of current industrial lithography techniques
- Complex patterned logic cells followed by advanced mask processing steps are still the dominant approach
- Necessity to counter the negative effects of significant regularity restrictions on logic density for advanced process nodes (32nm and below)

**Goals**
The Synaptic project targets the optimisation of manufacturability and the reduction of systematic variations in nanometer technologies through exploitation of regularity at the architectural, structural, and geometrical levels. We focus the research efforts on exploring and developing innovative design techniques and methodologies, along with associated CAD tools and logic cell libraries, which extract and preserve regularity, and automate the creation of regular compound cells which implement the functionality of the extracted templates.

**Metrics**
- Lithography analysis to verify the effects on conventional and RDR standard cells, as well as regular fabrics
  - establish the trade-off between area and yield
- Study of the effects of RDR’s on SRAM in terms of performance and manufacturability
  - definition of set of RDR’s, which allow manufacturability optimisation while remaining compatible with SRAM design rules

**Evaluation**
- ability to exploit step and repeat approaches employing complex logic cells and complex logic building blocks realised by regular layout patterns
  - reduces sensitivity to process variations, improving predictability of design performance and enabling tighter design margins
  - comprehensive early architecture exploration
- usage of regular architectures
  - automatically choosing a target architecture from a high level architectural library
  - identification of a small set of repeated functions and creation of a target fabric that is able to implement them

- definition of logic cell libraries targeted to design requirements
  - identification of complex cells
  - transistor-aware mapping to produce optimized Boolean expressions
- resynthesis of the design on the new library cells of complex cells
  - improve performance and its predictability
  - preserve and improve design regularity

- extend a cell library generator producing all standard library views (Liberty, LEF, GDS, etc) to support
  - the possibility to start from a Boolean description or from a transistor network described in SPICE format
  - the comparison of cells at different degrees of regularity
    - conventional standard-cells
    - regular (Restricted Design Rule - RDR) standard cells
    - regular fabrics
  - maximise predictability, manufacturability and reduce systematic variations though layout regularity

**Synaptic Cells Repository**
- W: 4 cols (920nm)
  - H: 9 tracks (1260nm)
  - Area: 1.1598 um²
- W: 4 cols (700nm)
  - H: 10 tracks (1400nm)
  - Area: 1.356 um²
- W: 4 cols (920nm)
  - H: 10 tracks (1600nm)
  - Area: 1.472 um²

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